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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,500	02/20/2004	Hideki Hirayama	10449-078001	7597

69713 7590 06/22/2007

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EXAMINER	
BIBBINS, LATANYA	

ART UNIT	PAPER NUMBER
2627	

MAIL DATE	DELIVERY MODE
06/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,500	HIRAYAMA, HIDEKI	
	Examiner	Art Unit	
	LaTanya Bibbins	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-10* is/are allowed.

6)☒ Claim(s) *1-3,5,6 and 9* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on May 30. 2007 has been entered.

Claim Objections

2. **Claims 9 and 10** are objected to because of the following informalities: claims 9 and 10 recite "the second **click** signal". Replacing "the second **click** signal" with "the second **clock** signal" is suggested. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5, 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobita et al. (US Patent Number 6,385,257 B1) in view of Hase et al. (US Patent Number 5,937,020).

Regarding claim 1, Tobita discloses a decoder for demodulating address information using a wobble signal, the decoder comprising: an analog PLL circuit for generating a second clock signal and synchronizing the second clock signal with the wobble signal based on a difference between the phase of the wobble signal and the phase of the second clock signal (see Figure 41 element 103 and the discussion in column 1 lines 39-49); and a demodulator, the analog PLL circuit, the demodulator sampling the wobble signal using the second clock signal to demodulate the address information (see Figure 41 and the discussion in column 1 lines 39-58).

Tobita fails to disclose, but Hase does disclose a digital PLL circuit for generating a first clock signal (see Figure 3 element 3) and a demodulator, connected to the digital PLL circuit and the analog PLL circuit and configured to be able to switch between the first and second clock signals (see the synchronizing clock generator and timing controller in Figure 3 elements 2 and 43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate both the analog and digital PLL's of Hase into the decoder of Tobita. One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings in order to achieve phase synchronization at high-speed upon initialization (provided by the analog PLL) and

achieve phase synchronization with high precision thereafter (provided by the digital PLL) as suggested by Tobita (column 10 lines 6-34).

Regarding claim 2, Tobita discloses a detection circuit for comparing the wobble signal and the second clock signal and detecting whether the second clock signal is synchronized with the wobble signal (see Figure 41 and the discussion in column 1 lines 39-49 and column 2 lines 34-37). Tobita fails to disclose but Hase discloses wherein the demodulator selects either the first clock signal or the second clock signal based on a detection result of the detection circuit (see the synchronizing clock generator and timing controller in Figure 3 elements 2 and 43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate selecting either the analog or digital PLL as taught by Hase in the decoder of Tobita. One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings in order to achieve phase synchronization at high-speed upon initialization (provided by the analog PLL) and achieve phase synchronization with high precision thereafter (provided by the digital PLL) as suggested by Tobita (column 10 lines 6-34).

Regarding claim 3, Hase discloses wherein the analog PLL circuit includes: a phase comparator for generating a phase difference signal in response to a difference between the phase of the wobble signal and the phase of a divisional clock signal generated by dividing the frequency of the second clock signal by a predetermined frequency dividing ratio (see Figure 15 elements 2014 and 2023 and the discussion in column 17 lines 6-25); a charge pump, connected to the phase comparator, for

generating current in accordance with the phase difference signal (see Figure 15 element 2024 and the discussion in column 17 lines 6-25); a low pass filter, connected to the charge pump, for generating voltage in accordance with the current of the charge pump (see Figure 15 element 2010 and the discussion in column 17 lines 6-25, specifically where the loop filter removes high-frequency components i.e. a low-pass filter); and a voltage-controlled oscillator, connected to the low pass filter, for oscillating in accordance with the voltage of the low pass filter and generating the second clock signal, wherein the detection circuit compares the wobble signal and the divisional clock signal and detects whether the second clock signal is synchronized with the wobble signal (see Figure 15 element 2011 and the discussion in column 17 lines 6-25).

Regarding claim 5, Hase discloses a first phase detector, connected to the digital PLL circuit, for detecting a phase inversion of the wobble signal based on the first clock signal (see Figure 15 element 2008); and a second phase detector, connected to the analog PLL circuit, for detecting a phase inversion of the wobble signal based on the second clock signal (see Figure 15 element 2014).

Regarding claim 6, Hase discloses a selector, connected to the first and second phase detectors, for selecting either the detected result of the first phase detector or the detected result of the second phase detector in accordance with a select signal (see the synchronizing clock generator and timing controller in Figure 3 elements 2 and 43).

Regarding claim 9, Tobita discloses wherein the analog PLL circuit generates the second clock signal as a reference signal (see Figure 41 where the analog PLL is

used as a reference signal for the phase comparator and the discussion in column 1 lines 43-46).

Allowable Subject Matter

5. Claims 7, 8, and 10 are allowed.

6. The following is an examiner's statement of reasons for allowance:

Regarding independent claim 7, none of the references of record, alone or in combination suggest or fairly teach a decoder for demodulating address information using a wobble signal including **a demodulator, connected to the digital PLL circuit, the analog PLL circuit, and the detection circuit, for sampling the wobble signal using the first clock signal to demodulate the address information when the select signal is inactive and for sampling the wobble signal using the second clock signal to demodulate the address information when the select signal is active.**

7. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding independent claim 11, none of the references of record, alone or in combination suggest or fairly teach a decoder for demodulating address information using a wobble signal, including all of the limitations of claim 1, wherein **the demodulator samples the wobble signal using the first clock signal until the second clock signal is synchronized with the wobble signal and samples the**

wobble signal using the second clock signal after the second clock signal is synchronized with the wobble signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaTanya Bibbins whose telephone number is (571) 270-1125. The examiner can normally be reached on Monday through Friday 7:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LaTanya Bibbins

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER